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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 044204-0308164

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on November 14, 2005

Signature: /Sachiko Y. Snedden/

Typed or printed name: Sachiko Y. Snedden

Application Number	Filed
09/847,981	May 2, 2001

First Named Inventor: Jason Seung-Min Kim

Art Unit	Examiner
2182	Schneider, Joshua D.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 55636
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Anthony G. Smyth/
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November 14, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

Attorney Docket: 044204-0308164

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kim, Jason Seung-Min
Application No.: 09/847,981
Filed: May 2, 2001

Confirmation No. : 5778
Group Art Unit.: 2182
Examiner: Schneider, Joshua D.

Title: METHOD FOR IMPLEMENTING SOFT-DMA (SOFTWARE BASED DIRECT MEMORY ACCESS ENGINE) FOR MULTIPLE PROCESSOR SYSTEMS

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pre-Appeal Brief Request for Review

This brief is submitted concurrently with a Notice of Appeal in the above-listed Application. The Notice of Appeal is filed in response to the Office Action mailed on July 12, 2005. An Advisory Action was mailed October 6, 2005 in response to an After Final Amendment filed by Applicant on September 12, 2005. A petition for a one month extension of time is filed herewith covering the period October 12, 2005 until present, November 12, 2005 having fallen on a Saturday.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8 and/or 1.10*

(When using Express Mail, the Express Mail label number is *mandatory;Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature

Date: November 14, 2005

SACHIKO Y. SNEDDEN
(type or print name of person certifying)

** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

REMARKS

Claims 1-9 are pending in the Application. In the Final Office Action ("FOA"), claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,884,027 to Garbus et al. ("Garbus") in view of "Structured Computer Organization" by Tanenbaum.

Applicant respectfully submits that Garbus does not teach or suggest all of the limitations in the claims and that Tanenbaum fails to cure the deficiencies of Garbus. Applicant also submits that new references introduced in the Advisory Action do not render the presently claimed invention obvious.

Garbus Does Not Teach Or Suggest All Limitations Of The Claims

In the Final Office Action, the Examiner acknowledged and agreed with Applicant's submission that Garbus does not teach, suggest or otherwise render obvious all of the limitations of the claims (FOA at page 2, second paragraph). However, the Examiner contends that such deficiency is "irrelevant as the rejection is an obvious rejection" (*Id.*). Applicant disagrees.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.

(MPEP 706.02(j) citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), emphasis added). As shown below, no other cited reference cures the deficiencies of Garbus. Therefore, the rejections of the claims under 35 U.S.C. § 103 are improper because Garbus combined with Tanenbaum, does not teach or suggest all the claim limitations.

Claim 1 requires, *inter alia*, a first processor coupled to a first bus, a second processor coupled to a second bus and an instruction memory coupled to the first bus and the second bus and having a software direct memory access (DMA) engine stored therein, wherein the software DMA engine is adapted to be executed by a processor of the first and second processors, the processor being coupled to the first bus and the second bus. The software DMA engine must be capable of transferring data directly between all of a plurality of resources, each of the plurality of resources being connected to at least one of the first bus and the second bus.

Garbus does not teach the required first and second processors or the instruction memory as recited in the claims. The Examiner suggests that Figure 2 teaches the recited first and second processors, nominating system 31 as second processor and PCI busses 17 and 19 as first bus and second bus, respectively (*see* FOA at page 2, second paragraph). However, Figure 3 of Garbus shows cited PCI-to-PCI bus bridge system 31 as consolidating "a high performance processor ... a PCI-to-PCI bus bridge 32, PCI bus-processor address translation unit, direct memory access (DMA) controller, memory controller, secondary PCI bus arbitration unit, inter-integrated circuit (I^2C) bus interface unit, advanced programmable interrupt (APIC) bus interface unit, and a messaging unit into a single system 31 which utilizes a local memory 33" (Garbus, col. 2, lines 9-22). Therefore, the characterization of Garbus' system 31 as teaching the second processor of claim 1 is factually incorrect because it conflicts with the explicit description in Garbus.

Furthermore, Garbus teaches DMA controllers 51a and 51b that refute Examiner's assignment of DMA functionality to system 31. The two DMA controllers 51a and 51b operate independently of local processor 34 to transfer data between ***local bus*** 41 and PCI busses 17 and 19, respectively; neither of DMA controllers 51a and 51b is coupled to both PCI bus 17 *and* PCI bus 19 (*see* Garbus, claim 6 and col. 3, lines 38-40). Therefore, DMA controllers 51a and 51b are incapable of transferring data directly between all of the plurality of resources, each of the plurality of resources being connected to at least one of the first bus and the second bus.

Nor is the Garbus local processor 34 coupled to a first bus and a second bus such that it could execute a DMA engine capable of transferring data directly between all of a plurality of resources connected to at least one of the first bus and the second bus. Garbus explicitly teaches that "[t]he local processor operates out of its own 32-bit address space and not PCI address space" (col. 2, lines 45-46). Furthermore, it would have been apparent to one skilled in the art that the "*functionally unmodified*" Intel 80960 JF processor 34 taught in the preferred Garbus embodiment has a single address/data bus and is thus incapable of being coupled to more than one bus (*see* Garbus at Figure 3 and at col. 2, lines 37-44). Therefore, Garbus cannot be said to teach or suggest a processor capable of executing a DMA engine as recited in claim 1.

Curiously, the FOA includes no allegation that any of the cited art teaches the required instruction memory having a software direct memory access (DMA) engine stored therein. As recited in claim 1, the instruction memory must be coupled to the first bus and the second bus. Local memory 34 of Garbus does not teach or suggest such limitations since it connects only to

local bus 41 and can communicate with bus 17 or bus 19 only through DMA controllers 51a and 51b (Garbus, Figure 3 and at col. 2, lines 45-46). Therefore, it cannot be said that Garbus teaches or suggests an instruction memory coupled to the first bus and the second bus.

As acknowledged by the Examiner, Garbus does not teach the required Software DMA engine stored in the instruction memory and adapted to be executed by a processor of the first and second processors, the processor being coupled to the first bus and the second bus. As shown below, the Examiner cites no other reference that teaches or suggests all the limitations associated with the recited software DMA engine.

Therefore, for at least the reasons provided, Garbus does not teach, suggest or otherwise render obvious all of the limitations of the claims.

Tanenbaum Does Not Cure The Deficiencies Of Garbus

Tanenbaum is offered in the FOA merely as support for the aphorism that "hardware and software are logically interchangeable" (page 5, lines 3-4). In the Advisory Action, Tanenbaum is specifically quoted as teaching the concept that "designers must decide what to put in each level" (Advisory Action at page 2). Nevertheless, Tanenbaum provides no substantive teachings related to the limitations of the present claims and cannot properly be used as a panacea to cure the deficiencies of Garbus. Garbus fatally lacks, *inter alia*, a first processor coupled to a first bus, a second processor coupled to a second bus, an instruction memory coupled to the first bus and the second bus and having a software direct memory access (DMA) engine stored therein, wherein the software DMA engine is adapted to be executed by a processor of the first and second processors, the processor being coupled to the first bus and the second bus.

Nothing in Tanenbaum teaches or suggests the missing instruction memory coupled to first and second busses. Nothing in Tanenbaum teaches or suggests how an Intel 80960 JF microprocessor can be coupled to the recited first and second bus in addition to a local bus. Tanenbaum does not teach software methods for implementing physical bus coupling in software or the software implementation of an instruction memory such that the instruction memory is coupled to first and second physical busses. Therefore, the rejections lack merit and should be withdrawn because no factual basis exists to support a rejection based on Garbus and Tanenbaum.

New References In The Advisory Action Are Ineffective In Supporting The Claim Rejections

In the Advisory action, the Examiner cites U.S. Patent No. 6,668,287 to Boyle et al. ("Boyle") and an Atmel Application Note ("Atmel") as contradicting Applicant's statement that no motivation existed to combine Tanenbaum with Garbus. However, neither Boyle nor Atmel cures the deficiencies of Garbus and Tanenbaum. Boyle merely teaches that, "by providing relatively simple hardware support, a fast processor has the ability to practice direct memory access in software without significantly slowing its operations" (col. 6, lines 14-17). Boyle provides a method directed to fast processors and recognizes performance degradation necessarily occurs; further Boyle teaches that some hardware is required. Atmel teaches the use of fast interrupts to implement a software simulation of DMA.

The new references do not teach or suggest a first processor coupled to a first bus, a second processor coupled to a second bus, an instruction memory coupled to the first bus and the second bus and having a software direct memory access (DMA) engine stored therein, wherein the software DMA engine is adapted to be executed by a processor of the first and second processors, the processor being coupled to the first bus and the second bus. Therefore, the new references do not cure the deficiencies of Garbus and are consequently irrelevant and merely cumulative of Tanenbaum.

CONCLUSION

For at least the reasons presented above, it is respectfully submitted that it is clear that the Examiner erred in rejecting the claims because the references do not teach every aspect of the claimed invention either explicitly or impliedly. Therefore, the rejections are improper and should be withdrawn. Further, the claims are believed to be in form for allowance, and such action is hereby solicited.

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